RC4227

Dual Precision Operational Amplifier

Features

- Very low noise
  Spectral noise density – 3.8 nV/√Hz
  1/F noise corner frequency – 2.7 Hz
- Very low VOS drift – 0.3 μV/Mo; 0.3 μV/˚C
- High gain – 500 V/mV
- High output drive capability – ±10V into 1K load
- High slew rate – 2.7 V/μS
- Wide gain bandwidth product – 8 MHz
- High common mode rejection ratio – 104 dB
- Low input offset voltage – 75 μV
- Low frequency noise – 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input offset current – 2.5 nA
- Industry standard pinout
- 8-Lead DIP

Description

The RC4227, a dual version of the OP-27, is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70˚) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75 μV max. Input bias current cancellation techniques are used to obtain ±45 nA max. input bias currents.

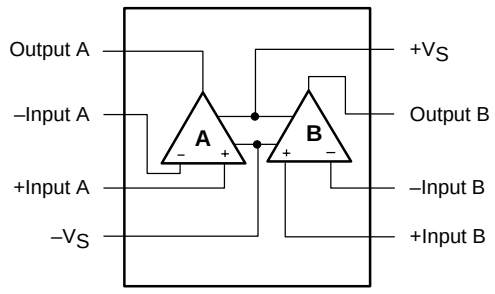
In addition to providing superior performance for audio frequency range applications, the RC4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 100 dB. A phase margin of 70˚ at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF[1]. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the RC4227 is achieved using precision amplifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow the RC4227 to be offered in an 8-pin mini-dip package and fit the industry standard dual op amp pinout.

Note:

1. By decoupling the load capacitance with a series resistor of 50Ω or more, load capacitances larger than 2000 pF can be accommodated.

Block Diagram



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Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				0.7	V
Internal Power Dissipation[3]				658	mW
$P_D T_A$ < 50°C	PDIP			468	mW
	CerDIP			833	
Output Short Circuit Duration		Indefinite			
Junction Temperature	PDIP			125	°C
	CerDIP			175	
Storage Temperature		-65		150	°C
Operating Temperature	RM4227B	-55		125	°C
	RC4227F/G	0		70	
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at	PDIP		6.25		mW/°C
	CerDIP		8.33		

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter			Min	Typ	Max	Units
θ_{JC}	Thermal resistance	CerDIP		45		°C/W
θ_{JA}	Thermal resistance	PDIP		160		°C/W
		CerDIP		150		°C/W

Electrical Characteristics

(V_S = ±15V, and $T_A \leq$ +25°C unless otherwise noted)

Parameters	Test Conditions	4227B/F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			20	150		30	180	μV
Long Term V_{OS} Stability[1]			0.3			0.4		μV/Mo
Input Offset Current			±2.5	±10		±5	±15	nA
Input Bias Current			±5	±15		±7.5	±25	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.08			0.08		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		3.8			3.8		$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.3			3.3		
	F_O = 1000 Hz		3.2			3.2		
Input Noise Current Density	F_O = 10 Hz		1.7			1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0			1.0		
	F_O = 1000 Hz		0.4			0.4		
Input Resistance (Diff. Mode)			5.0			4.0		MΩ
Input Resistance (Com. Mode)			2.5			2.0		GΩ
Input Voltage Range[2, 4]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	104	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	104	120		100	118		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	500	1000		400	800		V/mV
	V_{OUT} = ±10V, R_L = 1KΩ	400	800		300	600		
	V_{OUT} = ±1.0V V_S = ±4.0V, $R_L \geq 1.0k\Omega$	250	500		200	400		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		V
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate[2]	$R_L \geq 2.0k\Omega$	1.5	2.7		0.1	0.3		V/μs
Gain Bandwidth Product		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		70			70		Ω
Power Consumption	$R_L = \infty$		160	200		180	240	mW
Crosstalk		126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics

(V_S = ±15V, -55˚C ≤ T_A ≤ +125˚C unless otherwise noted)

Parameters	Test Conditions	4227B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			120	400	μV
Average Input Offset Voltage Drift[2]			0.3	3.5	μV/˚C
Input Offset Current			±10	±35	nA
Input Bias Current			±15	±45	nA
Input Voltage Range		±10	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	350	650		V/mV
Output Voltage Swing	R_L ≥ 2.0 kΩ	±11	±13.2		V
Power Consumption	R_L = ∞		200	280	mW

Notes:

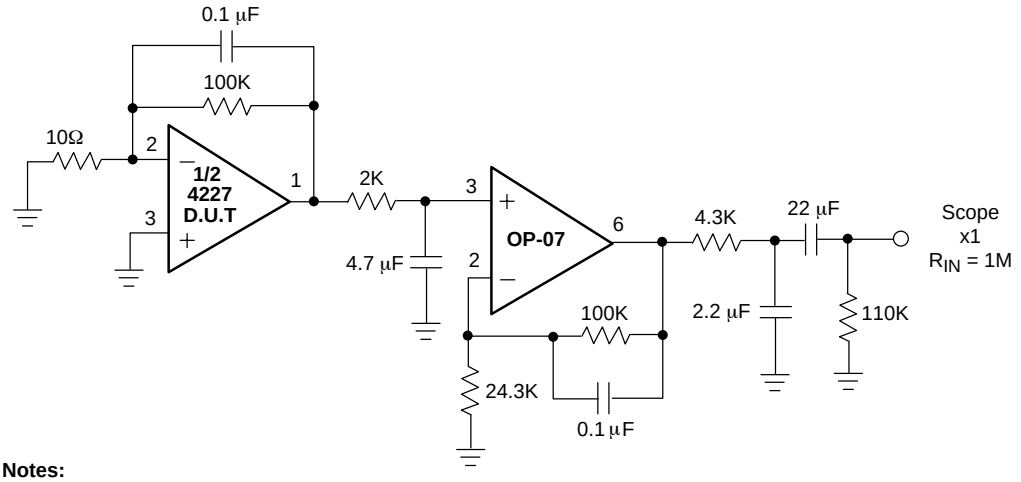
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70˚C unless otherwise noted)

Parameters	Test Conditions	4227F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.4		μV/°C
Input Offset Current			±8	±15		±10	±35	nA
Input Bias Current			±10	±30		±15	±45	nA
Input Voltage Range		±10	±11.8		±10	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	121		92	118		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	116		92	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	350	700		250	500		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.5		±11	±13.5		V
Power Consumption	R_L = ∞		180	240	200	280		mW

Typical Performance Characteristics



Notes:
1. Peak-to-peak noise measured in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents.
3. Voltage gain = 50,000.

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Figure 1. 0.1 Hz to 10 Hz Noise Test Circuit (1/2 Shown)

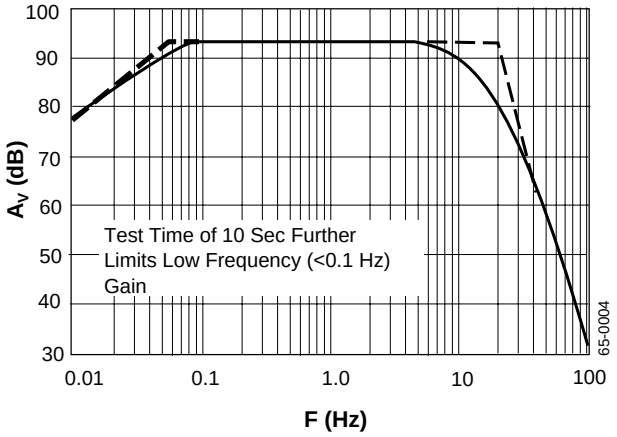


Figure 2. 0.1Hz to 10Hz Noise Gain vs. Frequency

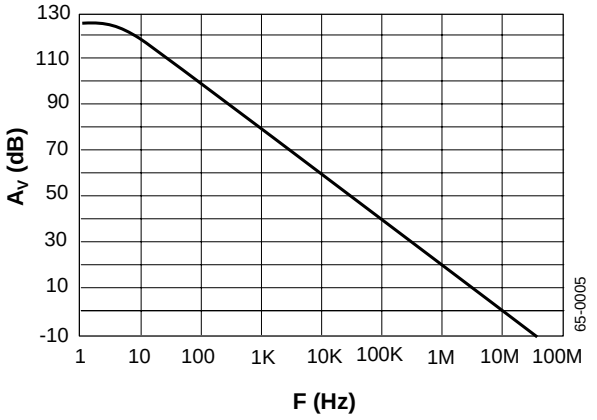


Figure 3. Open Loop Gain vs. Frequency

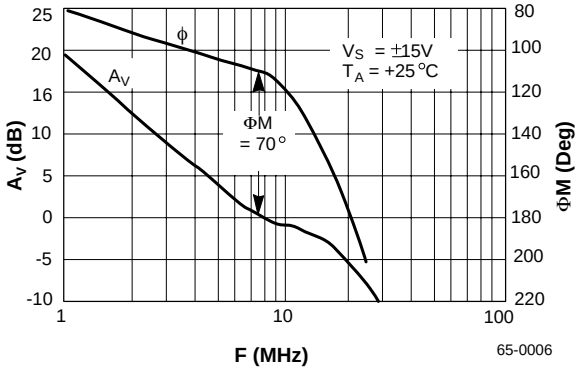


Figure 4. Gain, Phase Shift vs. Frequency

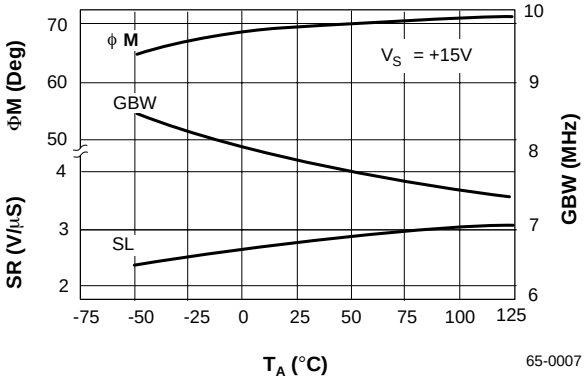


Figure 5. Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

Typical Performance Characteristics (continued)

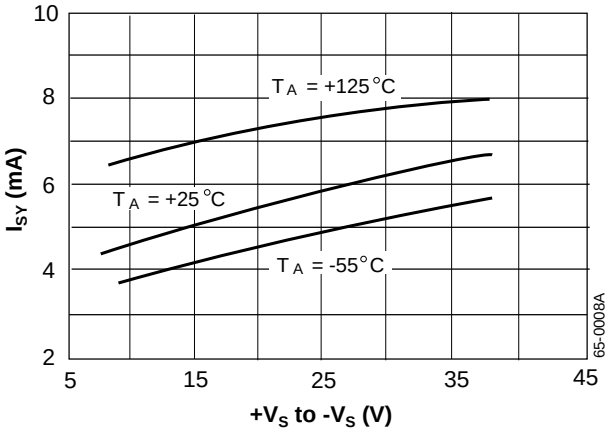


Figure 6. Supply Voltage vs. Total Supply Voltage

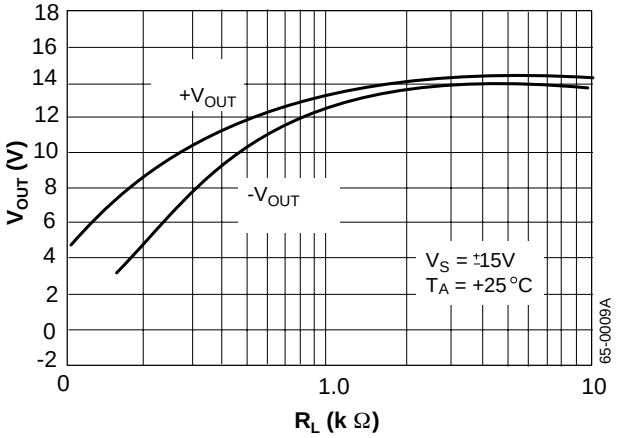


Figure 7. Maximum Output Swing vs. Load Resistance

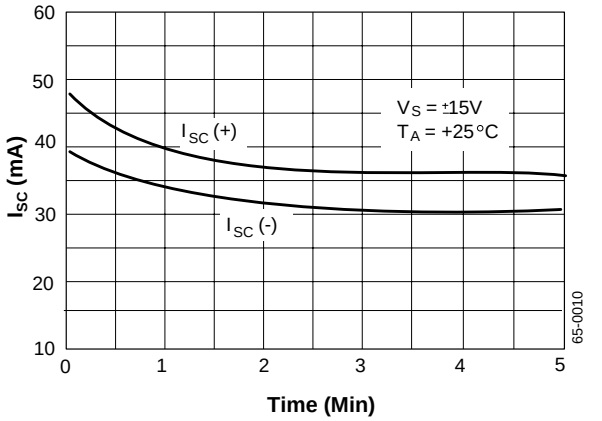


Figure 8. Short Circuit vs. Time

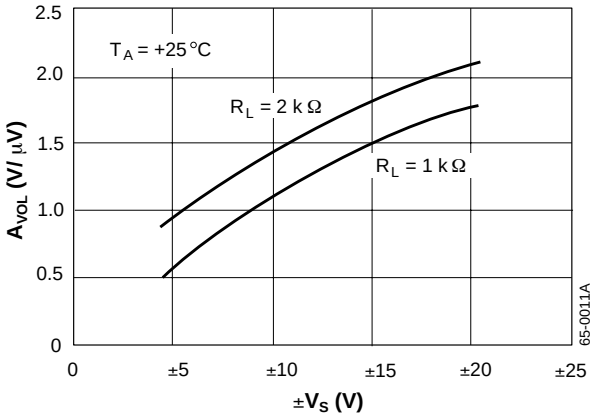


Figure 9. Open-Loop Gain vs. Total Supply Voltage

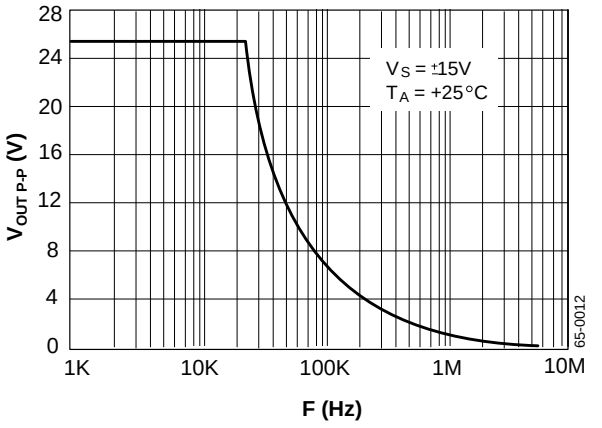


Figure 10. Maximum Undistorted Output vs. Frequency

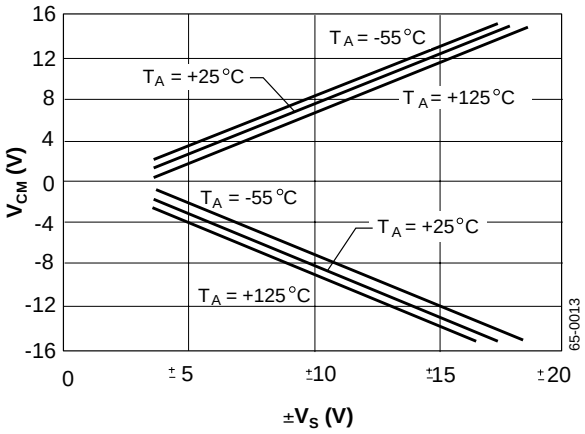


Figure 11. Common-Mode Input Range vs. Supply Voltage

Typical Performance Characteristics (continued)

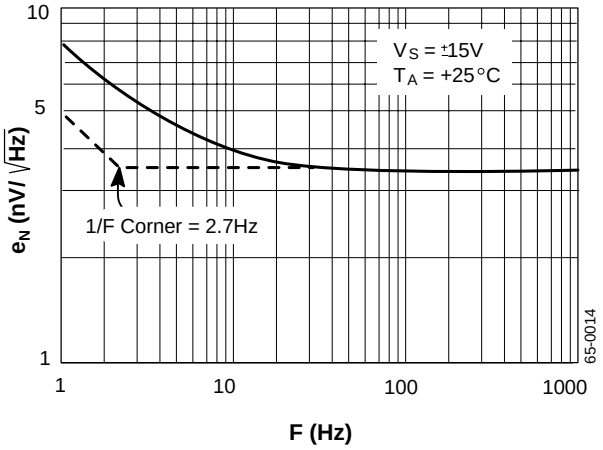


Figure 12. Input Noise Voltage Density vs. Frequency

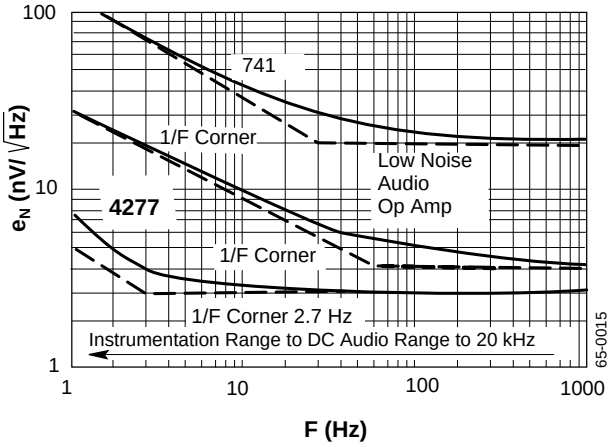


Figure 13. Op Amp Compensation Input Noise Voltage Density vs. Frequency

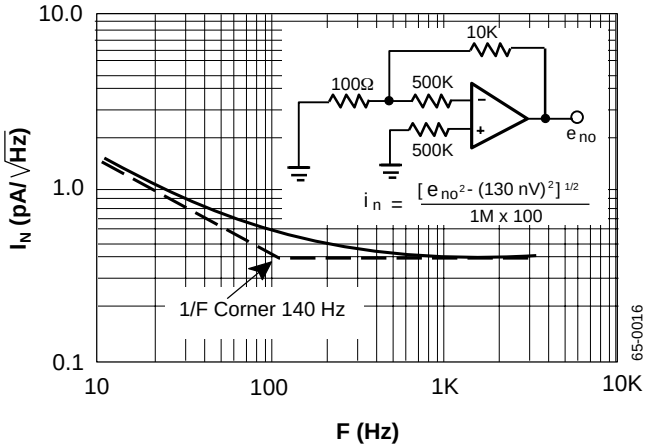
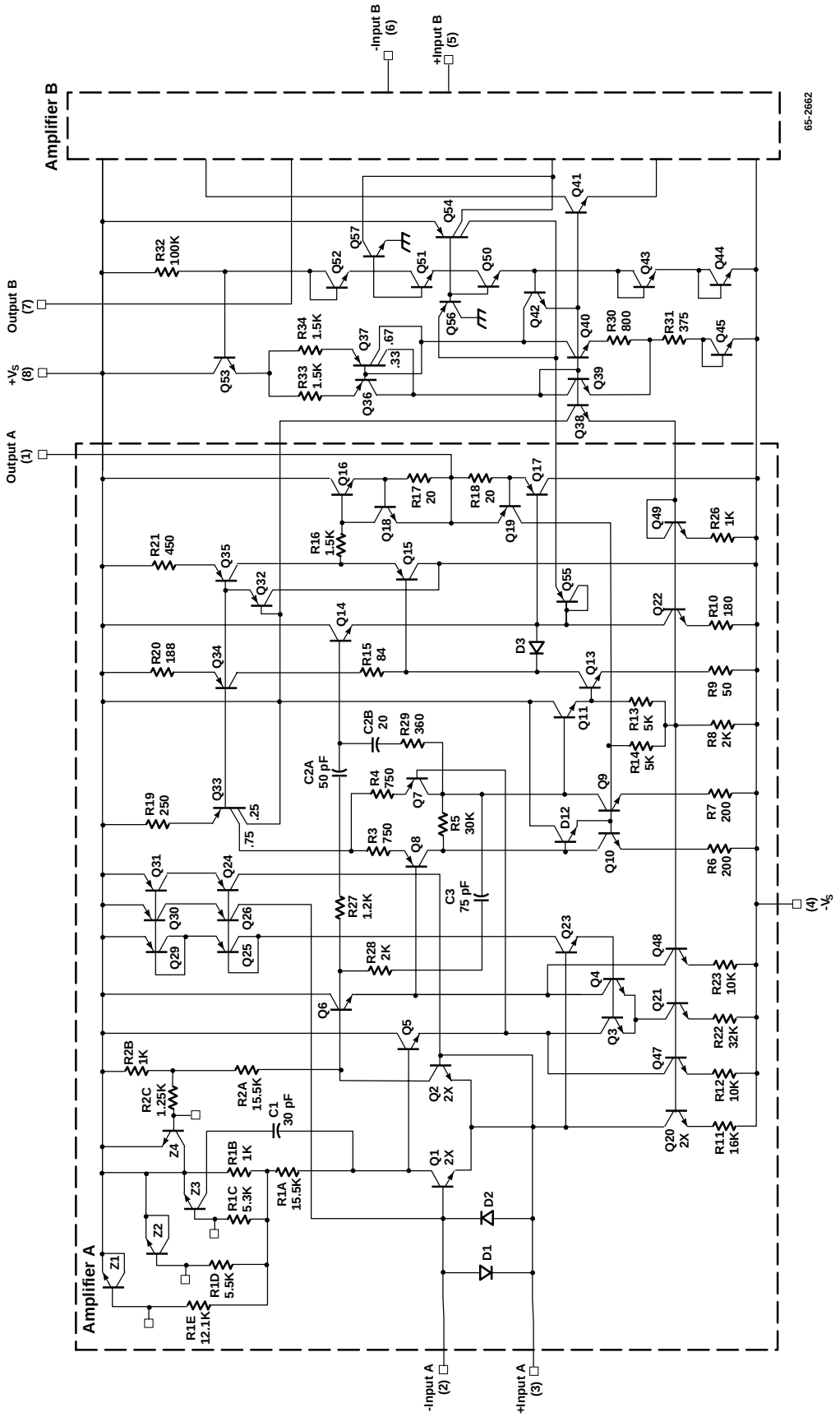


Figure 14. Input Noise Current Density vs Frequency

Simplified Schematic Diagram



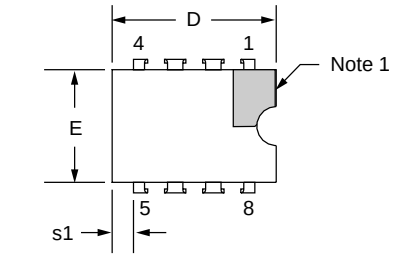
Mechanical Dimensions

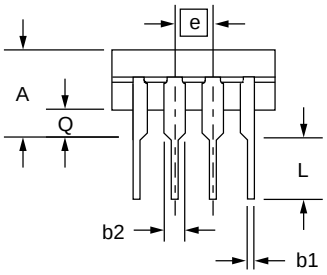
8-Lead Ceramic DIP Package

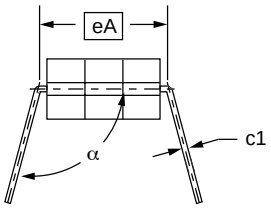
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.405	—	10.29	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
6. Applies to all four corners (leads number 1, 4, 5, and 8).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Six spaces.







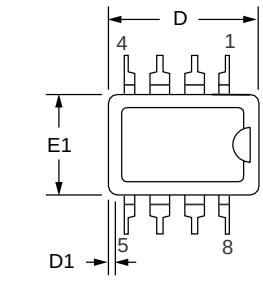
Mechanical Dimensions (continued)

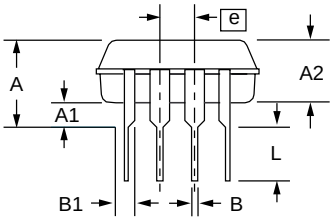
8-Lead Plastic DIP Package

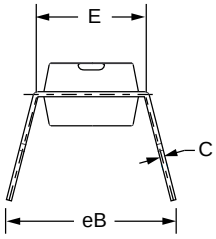
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4227FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4227GN	0° to +70°C	Commercial	8 Pin Plastic DIP
RM4227BD	-55°C to +125°C		8 Pin Ceramic DIP
RM4227BD/883[1]	-55°C to +125°C	Military	8 Pin Ceramic DIP

Note:

1. /883 suffix denotes MIl-STD-883, Par. 1.2.1 compliant device.